

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:
a semiconductor die having opposite surfaces;
a lead frame lying in a plane and having a strap cupped out of the plane of the lead frame to provide a nest, which is sized to receive the silicon die, an inner surface of the strap being in electric contact with one of the opposite surfaces of the semiconductor die received in the nest of the lead frame; and
a housing molded over and protecting the lead frame and the silicon die; the other surface of the semiconductor die being exposed for surface mounting connection with a support surface.
2. The semiconductor package defined in claim 1, wherein the lead frame extends along a longitudinal axis and has two laterally spaced rails bridged by the strap.
3. The semiconductor package defined in claim 1, wherein the semiconductor die is a MOSFET whose one surface has a source electrode attached to the inner surface of the strap, and the other surface of the silicon die has a drain electrode attachable to a printed circuit board.
4. The semiconductor package defined in claim 2, further comprising a gate electrode strap spaced laterally inwardly from the rails and spaced axially from the lateral strap, the gate electrode strap and the elongated sides having respective bottom surfaces which are coplanar with one another and with the other surface of the semiconductor die.

5. The semiconductor package defined in claim 4, wherein the gate electrode strap has a top surface in electric contact with a gate electrode of the MOSFET.

6. The semiconductor package defined in claim 3, further comprising solder bumps, which are distributed across either the top side electrode or the inner surface of the strap, for soldering the source electrode to the strap.

7. The semiconductor package defined in claim 3, further comprising conductive epoxy between the source electrode and the inner surface of the strap to provide electric contact therebetween.

8. The semiconductor package defined in claim 3, further comprising a polyamide tape having adhesive opposite surfaces which are attached to the source electrode and to the inner surface of the strap, respectively.

9. The semiconductor package defined in claim 2, wherein each of the elongated rails is continuous.

10. The semiconductor package defined in claim 2, wherein each of the elongated sides is segmented.

11. The semiconductor package device defined in claim 1, further comprising an least one other strap displaced out of the plane of the lead frame.

12. The semiconductor package device defined in claim 1, wherein the other surface of the semiconductor die extends so that it at least terminates in the same plane as a bottom surface of the housing.

13. A lead frame for a semiconductor die, the lead frame lying in a plane and having a plurality of coplanar sides, which define a nest sized to receive the semiconductor die, and a strap displaced out of the plane of the lead frame and extending across the nest to bridge two coplanar sides for positioning the semiconductor die in the nest so that a bottom surface of the semiconductor die, which faces away from the strap, is exposed for surface mounting connection.

14. The lead frame defined in claim 13, wherein the coplanar sides of the lead frame have respective bottom surfaces which are coplanar with the bottom surface of the semiconductor die.

15. The lead frame defined in claim 14, further having a housing molded over and protecting the lead frame and the semiconductor die; the bottom surfaces of the coplanar sides and of the semiconductor die being flush with or extend beyond a bottom surface of the housing.

16. A method for manufacturing a semiconductor package comprising the steps of:

providing an elongated lead frame lying in a plane;

cupping a strap from the plane of the lead frame, thereby providing a nest in the lead frame;

inserting a semiconductor die in the nest so that a bottom surface of the semiconductor die is exposed for surface mounting connection; and

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establishing electric contact between a top surface of the semiconductor die and an inner surface of the cupped strap.

17. The method defined in claim 16, further comprising the step of overmolding the lead frame with the semiconductor die with a plastic mold, thereby providing a housing which protects the lead frame and the semiconductor die.

18. The method defined in claim 16, wherein the semiconductor die is MOSFET whose top surface is the source electrode, the method further comprising the steps of attaching the top surface of the MOSFET to the inner surface of the cupped strap, and inverting the lead frame to provide a wire bond on the lead frame between the gate electrode of the MOSFET and a protrusion formed on the lead frame and extending into the nest after the semiconductor die has been mounted to the lead frame but before the overmolding of the lead frame.

19. The method defined in claim 17, further comprising the step of deflashing the molded lead frame.

20. The method defined in claim 17, further comprising the step of singulating the molded lead frame to form a plurality of frame segments each having a respective cupped strap and a respective semiconductor device, thereby producing a multiplicity of individual semiconductor packages.